

Key Feature

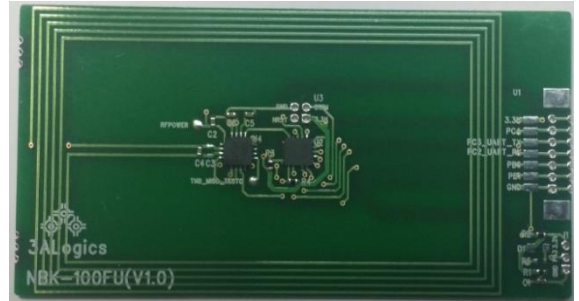
Frequency	13.56MHz	
Protocol	ISO/IEC 18092 (JIS 6319-4)	
Operating Temp.	-40 ~ 85°C	
Power	1.65 ~ 3.6V	
Host interface	- USART (2Port / GPIO) *Interface extension and changeable - GPIO (3Port)	
USART Speed	9600 ~115200 bps	
Host interface Protocol	N-Bridge Command / Protocol (proprietary)	
Board	PCB - FR4, 1.0T 32mm X 61mm X 1.75mm	
Antenna Size	5 turn, 31mm X 52mm L = 2.47μH	
NFC mode	Type 3 tag emulation *NFCIP-1 passive target	
Modulation	Load modulation	
Data rate	212 / 424kbps (Selective data rate)	
Microcontroller	STM8L101F3 (8bit Ultralow power)	
Memory	Type	Flash/EEPROM/RAM
	Size	8Kbyte/2Kbyte/1.5Kbyte

Key Application

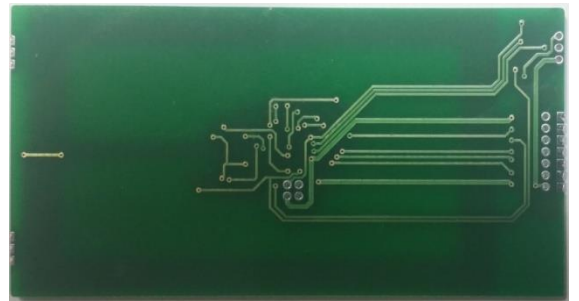
- Making connection (BT pairing, Wi-Fi setup)
- NFC Bridge Solution
(Providing RF interface to RF communicate between NFC Device and Target Device)
 - Embedded target device system
- NFC Energy Harvesting
 - Battery-less sensor, toy, ESL, ... etc
- NFC Firmware upgrade system
- Smart home appliances (Display-less)
or other applications with built-in microcontroller
- NFC Application (NFC Forum SIGs)
 - Health-care
 - Consumer electronics
- NBM-100A Target Application (Recommended)
 - ☞ Display-less device, Battery-less sensor, NFC Firmware upgrade system

Exterior

TOP

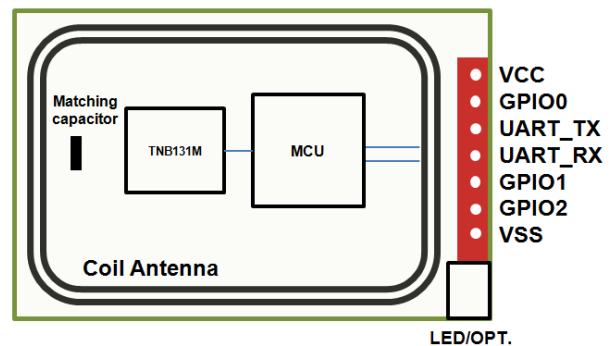


Bottom

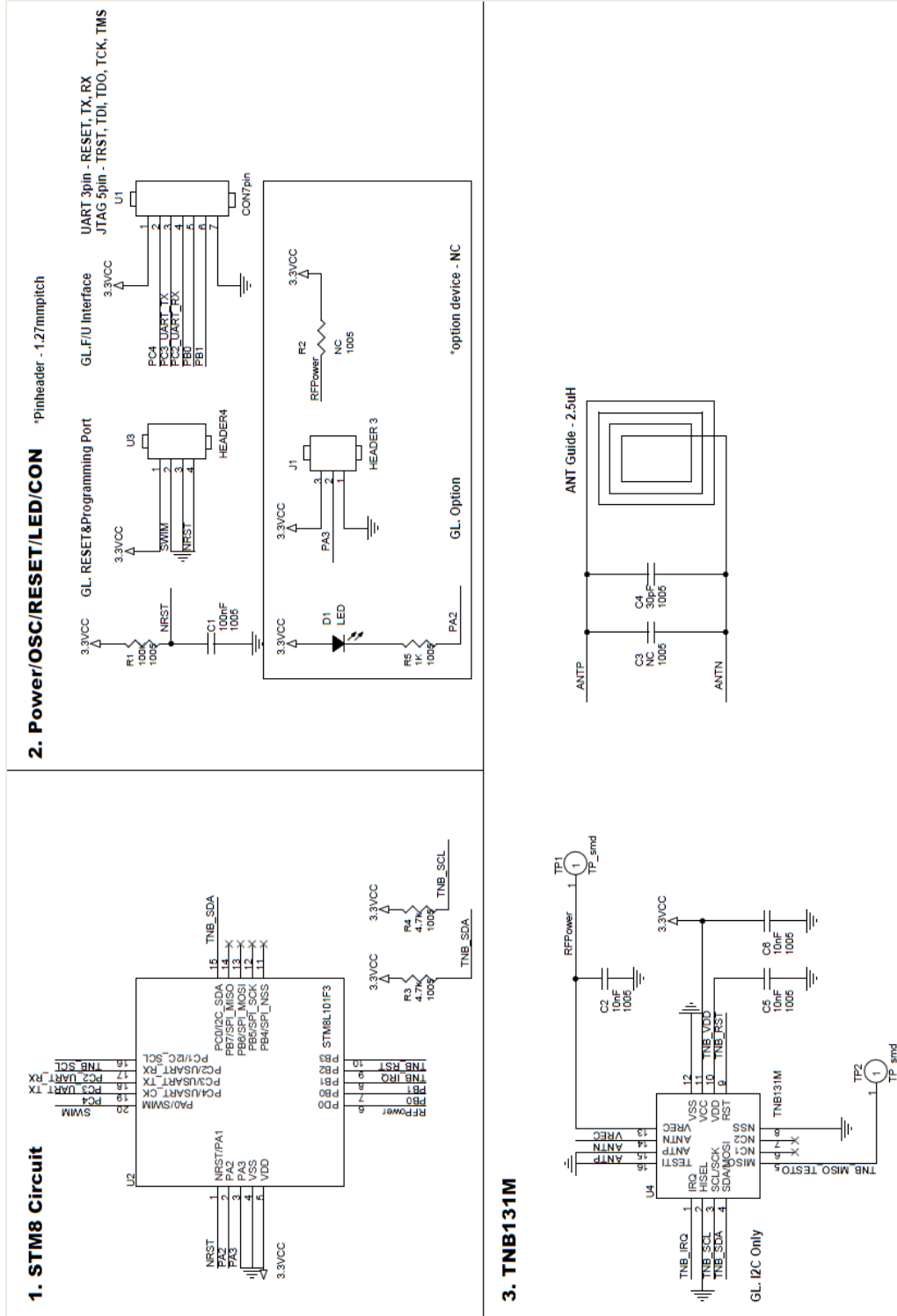


Block Diagram / Interface

Please see below block diagram for detailed information.

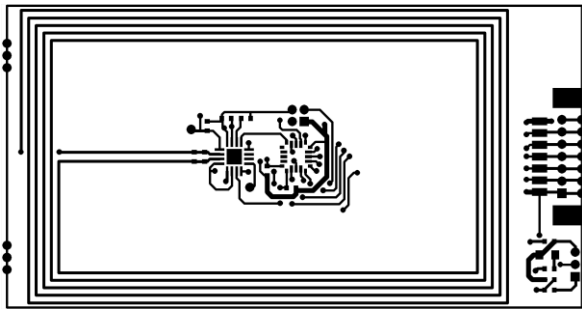


Schematic

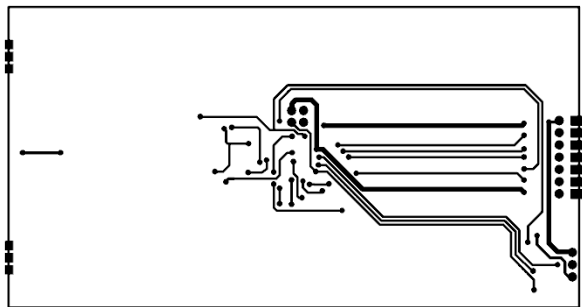


Gerber

TOP



Bottom



* 2 Type Size

Type1 -

Board	PCB - FR4, 1.0T 32mm X 61mm X 1.75mm
Antenna Size	5 turn, 31mm X 52mm L = 2.47μH

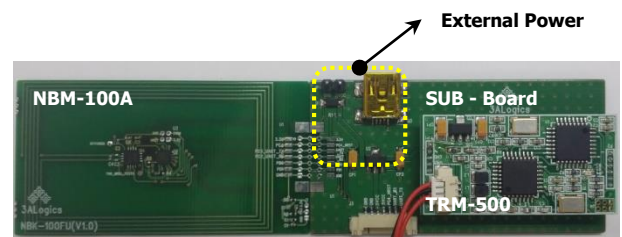
Type2 -

Board	PCB - FR4, 1.0T 32mm X 35mm X 1.75mm
Antenna Size	7 turn, 26.5mm X 34.5mm L = 2.94μH

NBM-100A Development KIT's

NBM-100A FU KIT

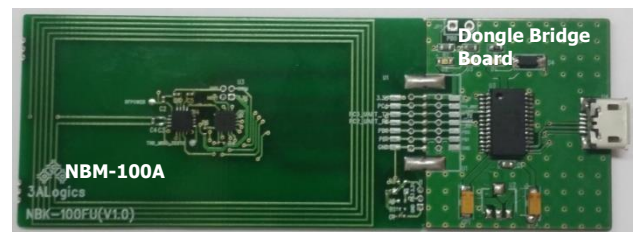
- Firmware Upgrade Development KIT
 - : NBM-100A
 - + SUB-Board
(NBM-100A & TRM-Series Bridge Board)
 - + TRM-500 / TRM-700
(3ALogics NFC R/W module)



☞ After the up-to-date Firmware Hex file is downloaded through server and run N-Bridge loader app. and Firmware of (NFC) TRM-500 is upgraded to the newest version by radio through NBM-100A on the Mobile phone.

NBM-100A Dongle KIT

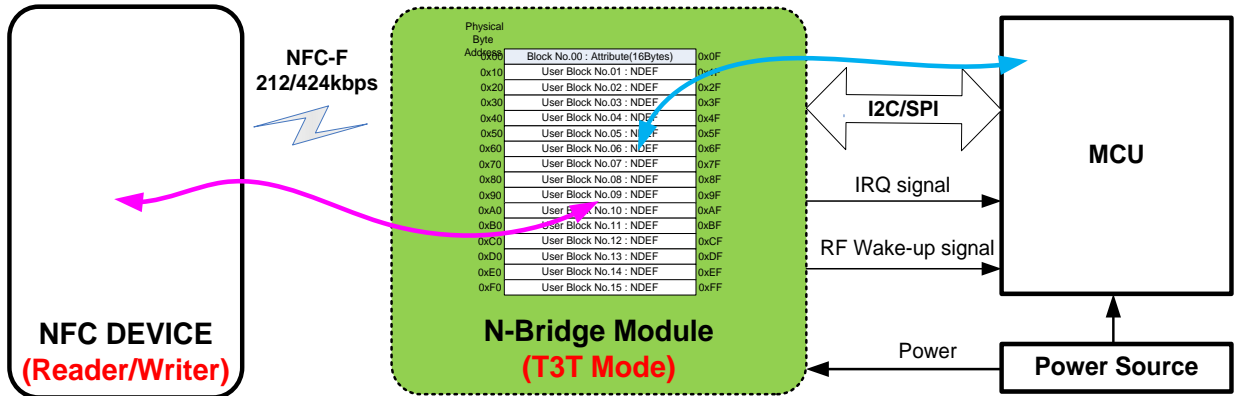
- PC Communication Development KIT
 - : NBM-100A
 - + N-bridge PC USB Con-Board



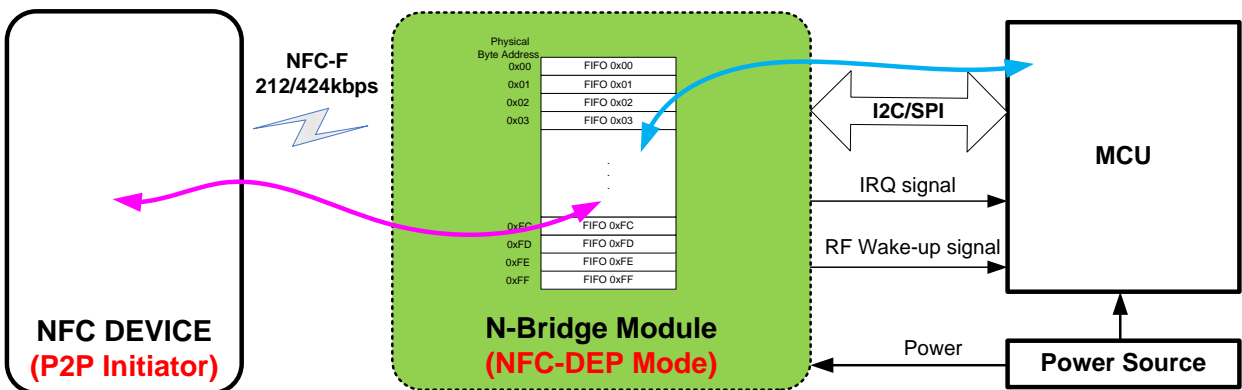
☞ Detailed operation and control of each mode is feasible by converting NBM-100A module into the different kinds of mode through PC.

TNB131M NFC Bridge Operating mode Architecture

T3T (Type 3 TAG mode) – Basic operation mode



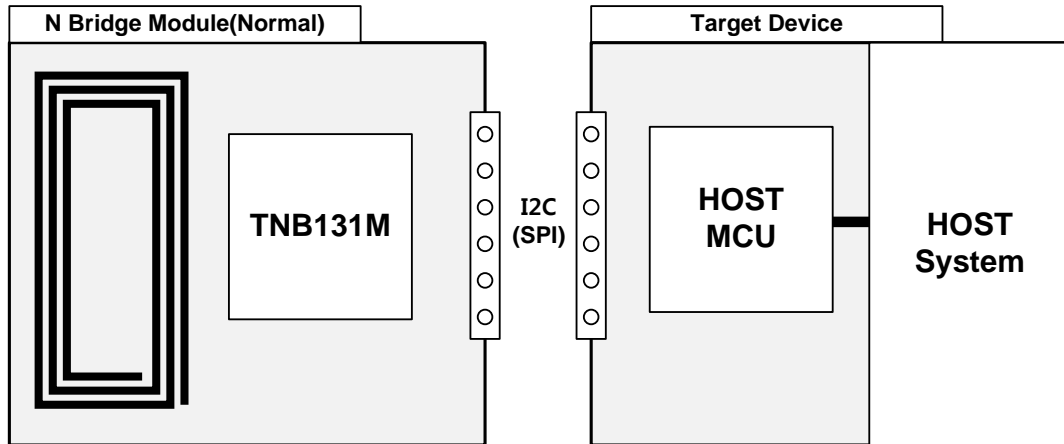
NFC-DEP (NFC Data Exchange Protocol mode) – Optional mode



- NFC Bridge Module, a passive operation, is operated by external NFC Device. (Master – NFC Device / Slave – N Bridge System)
- MCU is surely necessary to control N Bridge IC(TNB131M) to communicate with NFC device
- For a basic operation in the N Bridge Solution, NFC Device is operated by NFC R/W, N-Bridge module is operated by TAG.

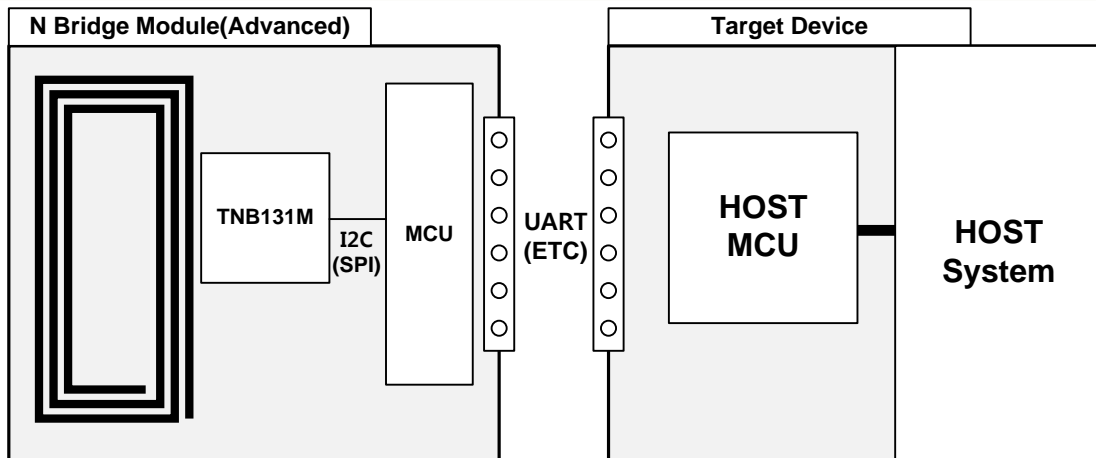
TNB131M NFC Bridge Module H/W Architecture

MBM-100N



• TNB131M Control Command – HOST Processor

MBM-100A



• TNB131M Control Command – Module MCU

- Condition to select TNB131M Module H/W
 - Host device MCU Spec.
 - Host device Interface
 - N Bridge module Program Size
 - N Bridge data storage Size
 - Antenna Size/Placement
 - ETC
 - * Program/data size is flexible case by case
(With different operation scenario and target application)

- Example 1 (I2C support MCU)
 - ☞ BT Simple pairing / Wi-Fi setup
Program size
: about 256Byte
- Example 2
 - ☞ Display-less device control
Program size
: about 2KByte ~ 8KByte

Electrical Specification

Operating condition range

Symbol	Parameter	MIN	TYP	MAX	UNIT
T_{op}	Operating temperature range	-40	+25	+85	°C
VCC	Main Power Supply / IO Power	1.65	3.3	3.6	V
f_{MASTER}	Master Clock Frequency	2	-	16	MHz

Current consumption

Symbol		Parameter	TEST Conditions	MIN	TYP	MAX	UNIT
MCU	PD	Power dissipation	T = 85°C	-	-	196	mW
			T = 125°C	-	-	49	mA
N Bridge	$I_{PWR-1.8V}$	Power Supply Current, VCC = 1.8V	Idle mode, T=25°C RF disable/Power on	45	50	60	uA
			Active mode, T=25°C RF field present Data Communication	I2C	145	165	240
	$I_{PWR-2.5V}$	Power Supply Current, VCC = 2.5V	Idle mode, T=25°C RF disable/Power on	70	75	90	uA
			Active mode, T=25°C RF field present Data Communication	I2C	265	285	315
	$I_{PWR-3.3V}$	Power Supply Current, VCC = 3.3V	Idle mode, T=25°C RF disable/Power on	100	110	125	uA
			Active mode, T=25°C RF field present Data Communication	I2C	335	370	405

Flash program memory

Symbol	Parameter	TEST Conditions	MIN	TYP	MAX	UNIT
V_{DD}	Operating voltage (all modes, r/w & erase)	$f_{MASTER} = 16\text{MHz}$	1.65	-	3.6	V
t_{prog}	Programming time for 1-or64-byte(block) erase/write cycles (on programmed byte)		-	6	-	ms
	Programming time for 1-or64-byte(block) write cycles (on erased byte)		-	3	-	ms
I_{prog}	Programming/erasing consumption	$T_A=25^\circ\text{C}, V_{DD}=3.0\text{V}$	-	0.7	-	mA
		$T_A=25^\circ\text{C}, V_{DD}=1.8\text{V}$	-		-	
t_{RET}	Data retention (program/data memory) after 10k erase/write cycles at $T_A = 85^\circ\text{C}$	$T_{RET}=55^\circ\text{C}$	20	-	-	years
	Data retention (data memory) after 300k erase/write cycles at $T_A = 125^\circ\text{C}$	$T_{RET}=85^\circ\text{C}$	1	-	-	

Standard I/O Pin DC characteristics

Symbol	Parameter	TEST Conditions	MIN	TYP	MAX	UNIT
V _{IL}	Input low level voltage	Standard I/Os	VSS-0.3	-	0.3 X VDD	V
		True open drain I/Os	VSS-0.3	-	0.3 X VDD	
V _{IH}	Input high level voltage	Standard I/Os	0.7 X VDD	-	VDD + 0.3	
		True open drain I/Os V _{DD} < 2V		-	5.2	
		True open drain I/Os V _{DD} ≥ 2V		-	5.5	
V _{hys}	Schmitt trigger Voltage hysteresis	Standard I/Os	-	200	-	
		True open drain I/Os	-	250	-	
I _{lkg}	Input leakage current	VSS ≤ V _{IN} ≤ VDD Standard I/Os	-	-	50	nA
		VSS ≤ V _{IN} ≤ VDD True open drain I/Os	-	-	200	
		PA0 with high sink LED Driver capability	-	-	200	
R _{PU}	Weak pull-up equivalent Resistor	V _{IN} = VSS	30	45	60	kΩ
C _{IO}	I/O pin capacitance		-	5	-	pF

Output driving current

Symbol	Parameter	TEST Conditions	MIN	TYP	MAX	UNIT	
Standard (high sink ports)	V _{OL}	Output low level voltage for an I/O pin	I _{IO} =2mA V _{DD} =3.0V	-	-	0.45	V
			I _{IO} =2mA V _{DD} =1.8V	-	-	0.45	V
			I _{IO} =10mA V _{DD} =3.0V	-	-	1.2	V
	V _{OH}	Output high level voltage for an I/O pin	I _{IO} =2mA V _{DD} =3.0V	V _{DD} -0.45	-	-	V
			I _{IO} =1mA V _{DD} =1.8V	V _{DD} -0.45	-	-	V
			I _{IO} =10mA V _{DD} =3.0V	V _{DD} -1.2	-	-	V
Open Drain (true open drain ports)	V _{OL}	Output low level voltage for an I/O pin	I _{IO} =3mA V _{DD} =3.0V	-	-	0.45	V
			I _{IO} =1mA V _{DD} =1.8V	-	-	0.45	V
IR (PA0 with high sink LED driver capability)	V _{OL}	Output low level voltage for an I/O pin	I _{IO} =20mA V _{DD} =2.0V	-	-	0.9	V

Document Control

Revision History

Date	Version	CR	HW version	Description
2014.04.28	0.1	01	0.1	0.1 version
2014.08.18	0.2	02	0.2	Up-version

Technical Support

- Protocol information
 - Datasheet TNB131M v1.1
 - User Manual N-Bridge v1.0
- Firmware code design (Case by Case)
 - Support Firmware example source code
- Android Application design (Case by Case)
 - * Demonstration Android Application
 - AnyRead NFC Tag Writer
- Customization Business
 - HW, FW&SW, Android App. Modification & Development

Legal Disclaimer

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